AMENDMENTS TO THE SPECIFICATION

1. Please replace paragraph [0002] with the following amended paragraph:

[0002] This application is related to the following co-pending U.S. Patent Applications, which are filed on the same day as this application, and which have a common assignee and a common inventor.

Serial Number	Docket Number	Title
10/759559	CNTR.2057	MICROPROCESSOR AND APPARATUS FOR PERFORMING FAST SPECULATIVE POP OPERATION FROM A STACK MEMORY
10/759564	CNTR.2229	MICROPROCESSOR AND APPARATUS FOR PERFORMING SPECULATIVE LOAD OPERATION FROM A STACK MEMORY
10/759489	CNTR.2233	MICROPROCESSOR AND APPARATUS FOR PERFORMING FAST POP OPERATION FROM RANDOM ACCESS CACHE MEMORY

2. Please replace paragraph [0011] with the following amended paragraph:

[0011] The present invention provides a variable latency cache memory. The cache memory includes a plurality of storage elements for storing stack memory data in a ~~first~~last-in-first-out (LIFO) manner. In one aspect, the cache memory distinguishes between requests for data in response to pop instructions and requests for data in response to load instructions. The cache memory speculates that pop data will be in the top cache line, and provides the pop data in a first number of clock cycles from the top cache line. The cache memory provides load data in a second number of clock cycles from any of the cache lines of the cache memory. The first number of clock cycles is less than the second number. That is, the pop data is provided faster than the load data because the pop data is provided speculatively before performing an address comparison to determine whether the pop data is actually present in the top cache line; whereas the load data is provided after performing an address comparison.